GUJARAT TECHNOLOGICAL UNIVERSITY

B. E. SEMESTER: VI

Electronics Engineering/Electronics &Communication Engineering/Electronics &Telecommunication

Subject Name: **VLSI Technology and Design**
Subject Code: **161004**

Teaching Scheme				Evaluation Scheme		
Theory	**Tutorial**	**Practical**	**Total**	**University Exam (Theory) (E)**	**Mid Sem Exam (Theory) (M)**	**Practical (I)**
4	0	2	6	70	30	50

Sr. No	Course Content	Total Hrs.
1.	**Introduction:** Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, ,computer aided design technology.	2
2.	**Fabrication of MOSFET :** Introduction, Fabrication Process flow: Basic steps, C-MOS n-Well Process, Layout Design rules, full custom mask layout design.	4
3.	**MOS Transistor:** The Metal Oxide Semiconductor (MOS) structure, The MOS System under external bias, Structure and Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances	8
4.	**MOS Inverters: Static Characteristics:** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement and Depletion type MOSFET load), CMOS Inverter	7
5.	**MOS Inverters Switching characteristics and Interconnect Effects :** Introduction, Delay-time definitions, Calculation of Delay times, Inverter design with delay constraints, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters	8
6.	**Combinational MOS Logic Circuits:** Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs)	5

7.	**Sequential MOS Logic Circuits :** Introduction, Behaviour of Bistable elements, The SR latch circuit, Clocked latch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop	4
8.	**Dynamic Logic Circuits :** Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques, High-performance Dynamic CMOS circuits	7
9.	**Chip I/P and O/P Circuits :** On chip Clock Generation and Distribution, Latch –Up and its Prevention	2
10.	**Design for testability :** Introduction, Fault types and models, Controllability and observability, Ad Hoc Testable design techniques, Scan –based techniques, built-in Self Test (BIST) techniques, current monitoring IDDQ test	3
11.	**Introduction to Programmable Logic Devices:** FPGA and CPLD	2

Text Book:

CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf Leblebici, TATA McGraw-Hill Pub. Company Ltd., Third Edition.

Reference Books:

(1) Basic VLSI Design By Pucknell and Eshraghian, PHI,3rd ed.
(2) Introduction to VLSI Systems by Mead C and Conway, Addison Wesley
(3) Introduction to VLSI Circuits & Systems – John P. Uyemura
(4) Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic

For Laboratory:

1. Minimum 9 practicals Based on VHDL/Verilog
2. Minimum 3 Practicals Based on Pspice/spice of MOSFET Characteristics
3. Minimum 2 Practicals on Layout Tools

VLSI design methodologies should be covered during Laboratory sessions.

Suggested List of Experiments

1. Introduction to programmable devices (FPGA, CPLD), Hardware Description Language (VHDL), and the use programming tool.
2. Implementation of basic logic gates and its testing.
3. Implementation of adder circuits and its testing.
4. Implementation 4 to 1 multiplexer and its testing.
5. Implementation of 3 to 8 decoder and its testing.
6. Implementation of J-K and D Flip Flops and its testing.
7. Implementation of sequential adder and its testing.
8. Implementation of BCD counter and its testing.
9. Implementation of two 8-bit multiplier circuit and its testing.
10. Simulation of CMOS Inverter using SPICE for transfer characteristic.
11. Simulation and verification of two input CMOS NOR gate using SPICE.
12. Implementation and simulation of given logic function using dynamic logic.
13. To generate layout for CMOS Inverter circuit and simulate it for verification.
14. To prepare layout for given logic function and verify it with simulations.

Mini Project

VHDL/Verilog based mini project with emphasis on design and implementation is compulsory